Refine Search

Your wildcard search against 10000 terms has yielded the results below.

Your result set for the last L# is incomplete.

The probable cause is use of unlimited truncation. Revise your search strategy to use limited truncation.

Search Results -

Terms	Documents
L6 same (second$)	28

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L7

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Thursday, March 16, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L7	L6 same (second$)	28	L7
L6	L4 same (first or primary)	40	L6
L5	L3 same l2	1	L5
L4	L3 same l1	172	L4
L3	configur$	1873527	L3
L2	(primary or first) adj1 l1	29	L2
L1	boundary adj1 scan adj1 (cell or chain)	769	L1

END OF SEARCH HISTORY

L5: Entry 1 of 1 File: USPT Jan 24, 2006

DOCUMENT-IDENTIFIER: US 6990618 B1
TITLE: Boundary scan register for differential chip core

CLAIMS:

1. An integrated circuit, comprising: a first boundary scan cell in a plurality of boundary scan cells, the plurality of boundary scan cells being configured for boundary scan testing of the integrated circuit, the first boundary scan cell being configured to receive a first input signal and output a first output signal and a second output signal, the first input signal comprising a differential signal as received by the first boundary scan cell; a second boundary scan cell in the plurality of boundary scan cells, the second boundary scan cell being configured to receive the first output signal of the first boundary scan cell, the second boundary scan cell being configured to output a third output signal and a fourth output signal; a third boundary scan cell in the plurality of boundary scan cells, the third boundary scan cell being configured to receive the third output signal of the second boundary scan cell, the third boundary scan cell being configured to output a fifth output signal and a sixth output signal; a core logic configured to receive the second output signal of the first boundary scan cell, the fourth output signal of the second boundary scan cell, and the sixth output signal of the third boundary scan cell, wherein the second output signal of the first boundary scan cell comprises a differential signal as received by the core logic; and a first input-output (I/O) node coupled to an input of the first boundary scan cell.

2. The integrated circuit of claim 1, further comprising: a level translator coupled between the first I/O node and the first boundary scan cell, wherein the level translator is configured to translate the first input signal from single ended to differential before being received by the first boundary scan cell.

3. The integrated circuit of claim 1, further comprising: a level translator coupled between the first boundary scan cell and the core logic, wherein the level translator is configured to translate the second output signal from single ended to differential before being received by the core logic.

4. The integrated circuit of claim 1, further comprising: a level translator coupled between the first boundary scan cell and the second boundary scan cell, wherein the level translator is configured to translate the first output signal of the first boundary scan cell from single ended to differential before being received by the second boundary scan cell.

8. A method of performing boundary scan testing, the method comprising: receiving a first differential signal in a first boundary scan cell in a plurality of boundary scan cells configured for performing boundary scan testing in a first integrated circuit, the plurality of boundary scan cells being coupled to a core logic of the first integrated circuit, the core logic of the first integrated circuit being configured to receive at least one differential signal.

14. An integrated circuit, comprising: means for receiving a first differential

signal in a first boundary scan cell in a plurality of boundary scan cells configured for performing boundary scan testing in a first integrated circuit, the plurality of boundary scan cells being coupled to a core logic of the first integrated circuit, the core logic of the first integrated circuit being configured to receive at least one differential signal.

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L7: Entry 11 of 28 File: USPT Feb 13, 2001

DOCUMENT-IDENTIFIER: US 6188241 B1
TITLE: Microcontroller having a block of logic configurable to perform a selected logic function and to produce output signals coupled to corresponding I/O pads according to a predefined hardware interface

Detailed Description Text (11):
Test/program core 30 is coupled to I/O pads 40 and to CLB 24. Test/program core 30 provides support for Joint Test Action Group (JTAG) boundary-scan testing of the circuitry of microcontroller 20. In accordance with well known JTAG boundary scan techniques, a boundary scan cell is associated with each I/O pad of microcontroller 20. The boundary scan cells are controlled by test/program core 30. In a normal operating mode, the boundary scan cells do not impede signals flowing to or from microcontroller 20 circuitry. In a test mode, test/program core 30 configures the boundary scan cells to form a serial "scan chain", and receives testing signals from an external device via I/O pads 40. Input values, received via a first I/O pad 40, are shifted through the scan chain, then applied to input signal lines of microcontroller 20. Output values, produced by output signal lines of microcontroller 20, are captured by a number of the boundary scan cells and shifted out through the scan chain and a second I/O pad 40. Test/program core 30 preferably provides support for JTAG boundary-scan testing in accordance with IEEE Standard 1149.1-1990.

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